WHAT IS CLAIMED IS:

1. A magnetic memory, comprising:

an array of magnetic memory cells; and

a control circuit configured to receive data, sort the received data to obtain unchanged data and ECC encoded data, and store the unchanged data and the ECC encoded data in the array of magnetic memory cells.

2. The magnetic memory of claim 1, wherein the control circuit is configured to evaluate sections of the array of magnetic memory cells and organize the sections into groups based on fault probabilities of the sections.

3. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into zero fault sections and usable fault sections.

4. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into zero fault sections and usable fault sections, and store the unchanged data in the zero fault sections and the ECC encoded data in the usable fault sections.

5. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into sections comprising zero fault sections and the unchanged data comprises fault intolerant data stored in the zero fault sections.

6. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into sections comprising usable fault sections and the ECC encoded data comprises fault intolerant data stored in the usable fault sections.

7. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into sections comprising usable fault sections and the unchanged data comprises fault tolerant data stored in the usable fault sections.

8. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into multiple groups of usable fault sections and assign a corresponding error correction code to each group of the multiple groups of usable fault sections.

9. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into zero fault sections, usable fault sections and heavy fault sections that are remapped into the zero fault sections and the usable fault sections.

10. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into sections comprising zero fault sections, and provide pointers for a sequence of the zero fault sections.

11. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into sections comprising zero fault sections and provide non-destructive reads in the zero fault sections.

12. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into sections comprising usable fault sections and provide destructive reads in the usable fault sections.

13. The magnetic memory of claim 1, wherein the control circuit is configured to organize the array of magnetic memory cells into zero fault

sections and usable fault sections, and swap usable fault sections with zero fault sections based on number of accesses during a predetermined period.

14. The magnetic memory of claim 1, wherein the control circuit is configured to ECC encode data using a Reed Solomon error correction code.

15. The magnetic memory of claim 1, wherein the control circuit is configured to ECC encode data using a BCH error correction code.

16. A magnetic memory, comprising:

an array of magnetic memory cells; and

a control circuit configured to divide the array of magnetic memory cells into zero fault sections and usable fault sections, receive data, and sort the received data into the zero fault sections and usable fault sections based on predetermined criteria.

17. The magnetic memory of claim 16, wherein the control circuit is configured to sort the received data based on fault tolerances of the received data.

18. The magnetic memory of claim 16, wherein the control circuit is configured to sort the received data based on speed requirements for accessing the received data in the array of magnetic memory cells.

19. The magnetic memory of claim 16, wherein the control circuit is configured to sort the received data based on frequency of accessing the received data in the array of magnetic memory cells.

20. The magnetic memory of claim 16, wherein the control circuit is configured to sort the received data into fault tolerant data and fault intolerant data and store the fault tolerant data in the array of magnetic memory cells and store the fault intolerant data in the zero fault sections.

21. The magnetic memory of claim 16, wherein the control circuit is configured to sort the received data into fault tolerant data and fault intolerant data and store at least some of the fault tolerant data in the zero fault sections of the array of magnetic memory cells.

22. The magnetic memory of claim 16, wherein the control circuit is configured to sort the received data into fault tolerant data and fault intolerant data and ECC encode at least some of the fault intolerant data and store at least some of the ECC encoded data in the usable fault sections.

23. The magnetic memory of claim 16, wherein the control circuit is configured to provide destructive reads in the zero fault sections and the usable fault sections.

24. The magnetic memory of claim 16, wherein the control circuit is configured to provide non-destructive reads in the zero fault sections.

25. A magnetic memory, comprising:

an array of magnetic memory cells;

means for dividing the array of magnetic memory cells into groups of sections; and

means for providing unchanged data and ECC encoded data for storage in the groups of sections.

26. The magnetic memory of claim 25, wherein the means for dividing the array of magnetic memory cells comprises evaluating magnetic memory cells in sections of the array of, magnetic memory cells; and calculating a fault probability for sections in the array of magnetic memory cells.

27. The magnetic memory of claim 25, wherein the means for providing unchanged data and ECC encoded data comprises a control circuit configured to

sort received data for storage into the groups of sections and pass selected received data to an ECC unit.

28. A method for storing data in an array of magnetic memory cells, comprising:
selecting received data for encoding;
encoding the selected data with an ECC scheme;
storing the ECC encoded data in the array of magnetic memory cells; and
storing some received data as received in the array of magnetic memory cells.

29. The method of claim 28, comprising dividing the array of magnetic memory cells into sections comprising sections that store received data as received and sections that store ECC encoded data; and wherein encoding the selected data comprises selecting one ECC scheme from a group of ECC schemes.

30. The method of claim 28, comprising dividing the array of memory cells into sections comprising multiple groups of usable fault sections and providing multiple ECC schemes that correspond to the multiple groups of usable fault sections, wherein encoding the selected data comprises encoding the selected data with one of the multiple ECC schemes and storing the ECC encoded data comprises storing the ECC encoded data in the group of usable fault sections corresponding to the one of the multiple ECC schemes.